In the Claims

Claim 1 (previously presented): A semiconductor device comprising:

a crystalline layer separated from a substrate by a first insulative material; the crystalline layer comprising silicon/germanium;

a floating charge trapping media over the crystalline layer;

a pair of source/drain regions proximate the charge trapping media and extending into the crystalline layer such that at least a portion of the source/drain regions are within the crystalline layer; the portion of the source/drain regions within the crystalline layer being contained within a single crystal of the silicon/germanium;

a second insulative material over the charge trapping media; and

a control gate over the second insulative material.

Claim 2 (original): The device of claim 1 wherein the charge trapping media is a floating gate comprising conductively doped silicon.

Claim 3 (original): The device of claim 2 wherein the second insulative material comprises ONO.

Claim 4 (original): The device of claim 1 wherein the charge trapping media is a floating plate.

Claim 5 (original): The device of claim 4 wherein the second insulative material comprises ONO.

Claim 6 (original): The device of claim 4 wherein the second insulative material comprises a high k dielectric material.

Claim 7 (original): The device of claim 4 wherein the floating plate comprises silicon enriched oxide.

Claim 8 (original): The device of claim 4 wherein the floating plate comprises silicon enriched nitride.

Claim 9 (previously presented): The device of claim 1 wherein the silicon/germanium comprises from about 10 to about 60 atomic percent germanium.

Claim 10 (original): The device of claim 1 wherein the crystalline layer is polycrystalline.

Claim 11 (original): The device of claim 1 wherein the crystalline layer is monocrystalline.

Claim 12 (original): The device of claim 1 wherein the crystalline layer has a relaxed crystalline lattice, and further comprising a strained crystalline lattice layer between the relaxed crystalline lattice and the charge-trapping media.

Claim 13 (original): The device of claim 12 wherein the strained crystalline lattice includes silicon.

Claim 14 (original): The device of claim 12 wherein the strained crystalline lattice includes silicon and germanium.

Claim 15 (original): The device of claim 1 wherein the source/drain regions are n type regions.

Claim 16 (original): The device of claim 1 wherein the substrate comprises a semiconductive material.

Claim 17 (original): The device of claim 1 wherein the substrate comprises glass.

Claim 18 (original): The device of claim 1 wherein the substrate comprises aluminum oxide.

Claim 19 (original): The device of claim 1 wherein the substrate comprises silicon dioxide.

Claim 20 (original): The device of claim 1 wherein the substrate comprises a metal.

Claim 21 (original): The device of claim 1 wherein the substrate comprises a plastic.

Claim 22 (previously presented): A memory device comprising the semiconductor device of claim 1.

Claim 23 (previously presented): A logic device comprising the semiconductor device of claim 1.

Claims 24-50 (cancelled).